REMARKS

In the Office Action mailed May 28, 2008 the Office noted that claims 10-16 were pending and rejected claims 10-16. No claims have been amended, no claims have been canceled, claim 17 has been added, and, thus, in view of the foregoing claims 10-17 remain pending for reconsideration which is requested. No new matter has been added. The Office's rejections are traversed below.

REJECTIONS under 35 U.S.C. § 102

Claims 10-12, 15 and 16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Van Hoof, U.S. Patent No. 7,080,238. The Applicants respectfully disagree and traverse the rejection with an argument.

On pages 2 and 3 of the Office Action, it is asserted that Van Hoof, col. 3, line 60 through col. 4, line 4 disclose "the initial operation step (6a) of the first operation is executed on the first context (3) at a first stage (2a), the following operation step (6b) of the first operation is executed on the first context (3) at a second stage (2b), and the initial operation step (7a) of the second operation is executed on the first context at the second stage (2b)," as in claim 10.

However, Van Hoof, col. 5, lines 6-14 states

> According to one embodiment of the invention, the contexts in the context pool 38 are processed in a round-robin fashion. According to this embodiment, the

> sub-processor 40 preferably processes **each context for an allotted context processing time, such as, for example, one clock cycle**, and performs a context switch for processing a next available context in the context pool after the allotted context processing time has expired. [Emphasis added]

Van Hoof, col. 5, lines 27-34 state

> The internal pipeline architecture of the stage sub-processor 40 preferably allows the concurrent processing of various instructions **for processing a context within each stage. In processing an instruction for a particular context, the sub-processor executes multiple operations, such as, for instance, an instruction fetch, instruction decode, execution, and memory access.** Each operation is preferably executed in internally pipelined stages of the sub-processor 40. [Emphasis added]

Thus, in Van Hoof, as a context is processed within a single stage and each stage is processed within a single clock cycle, it thus follows that all operation steps (i.e. operations as in Van Hoof) of an operation (i.e. instruction as in Van Hoof) are performed before the context is passed to the next stage.

In contrast, in the present claims, at a second stage of a following operation step of the first operation is performed on the context. Again, in Van Hoof, all the operation steps of an operation are performed within a single stage. Thus, Van Hoof does not disclose "the following operation step (6b) of the first operation is **executed on the first context (3) at a second stage** (2b)," (emphasis added) as in claim 10.

For at least the reasons discussed above, claim 10 and the claims dependent therefrom, are not anticipated by Van Hoof.

As discussed above, each instruction of Van Hoof and

the operations within it are executed in a single stage. Therefore, Van Hoof cannot disclose "the processor is arranged so that the following operation step (6b) of the first operation is presented to a programmer as being executed at the first stage (2a)," as in claim 15. In Van Hoof, the following stage would always be a different instruction, therefore the presentation to the programmer would always appear to be executes in a first stage and thus the presentation would not need to be altered.

Withdrawal of the rejections is respectfully requested.

REJECTIONS under 35 U.S.C. § 103

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being obvious over Van Hoof in view of Wallace, *Thread Multiple Path Execution*. The Applicants respectfully disagree and traverse the rejection with an argument.

Wallace adds nothing to the deficiencies of Van Hoof as applied against the independent claim. Therefore, Van Hoof and Wallace, taken separately or in combination, fail to render obvious the features of claims 13 and 14.

Withdrawal of the rejections is respectfully requested.

NEW CLAIM

Claim 17 is new. Support for the claim may be found, for example, on page 3 lines 23-25 of the Specification. The Applicants submit that no new matter has been added by the

addition of claim 17. The prior art fails to disclose at each clock cycle, the first context is unconditionally moved to a next stage.

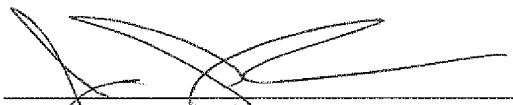
SUMMARY

It is submitted that the claims satisfy the requirements of 35 U.S.C. §§ 102 and 103. It is also submitted that claims 10-17 continue to be allowable. It is further submitted that the claims are not taught, disclosed or suggested by the prior art. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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